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DEC 23 2002

TRANSMITTAL OF FORMAL DRAWINGS

Docket No.
BUR920010217US1

In Re Application Of: Corbin et al.

Serial No.	Filing Date	Confirmation No.	Examiner	Art Unit
10/065,503	10/25/02			

Invention: **TESTING LOGIC AND EMBEDDED MEMORY IN PARALLEL**

Address to:
Assistant Commissioner for Patents
Washington, D.C. 20231

Transmitted herewith are:

3 sheets of formal drawing(s) for this application.

☒ Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).

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Dated: 12/11/2002

I certify that this document and attached formal drawings are being deposited on 12/16/02 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Pat Blair

Signature of Person Mailing Correspondence

PAT BLAIR

Typed or Printed Name of Person Mailing Correspondence

FIG. 1

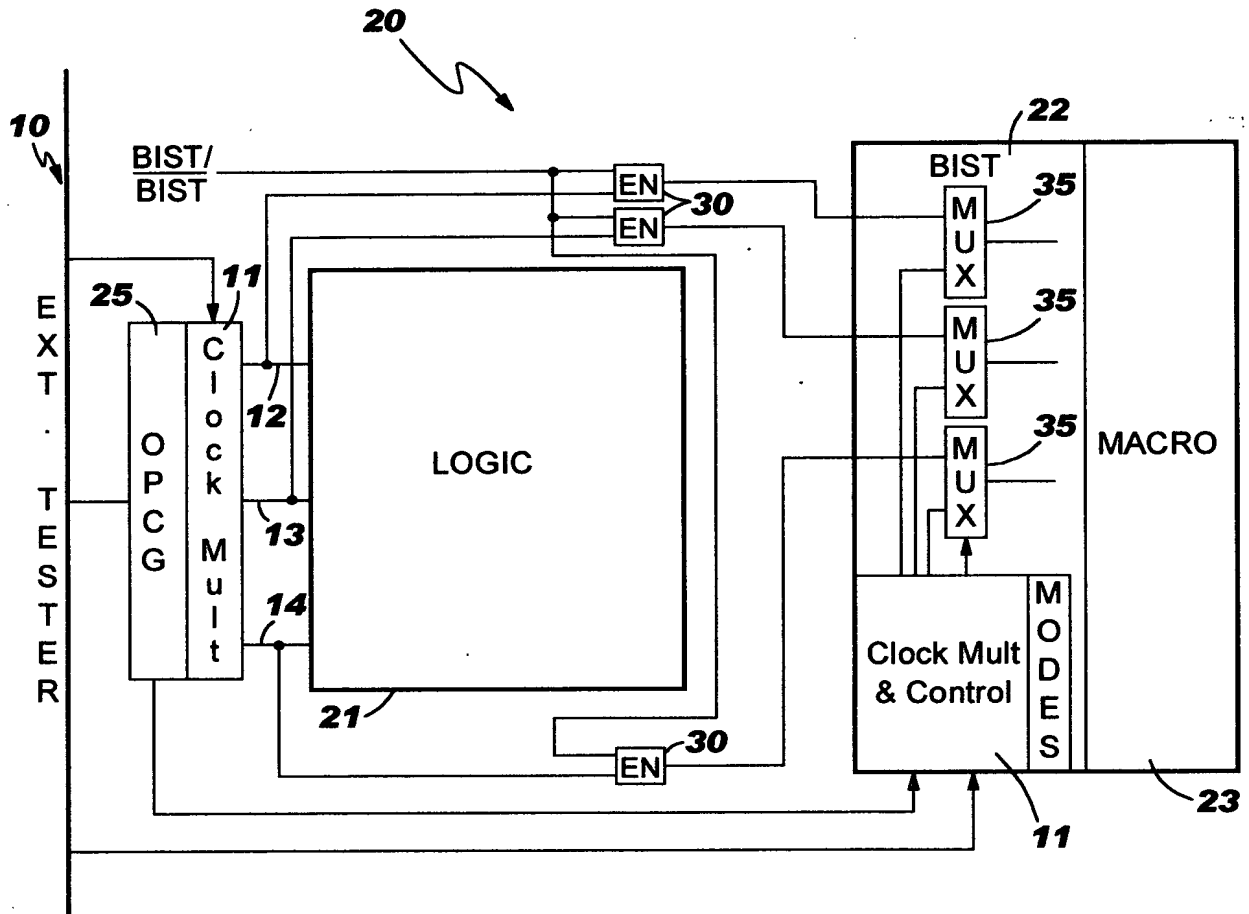
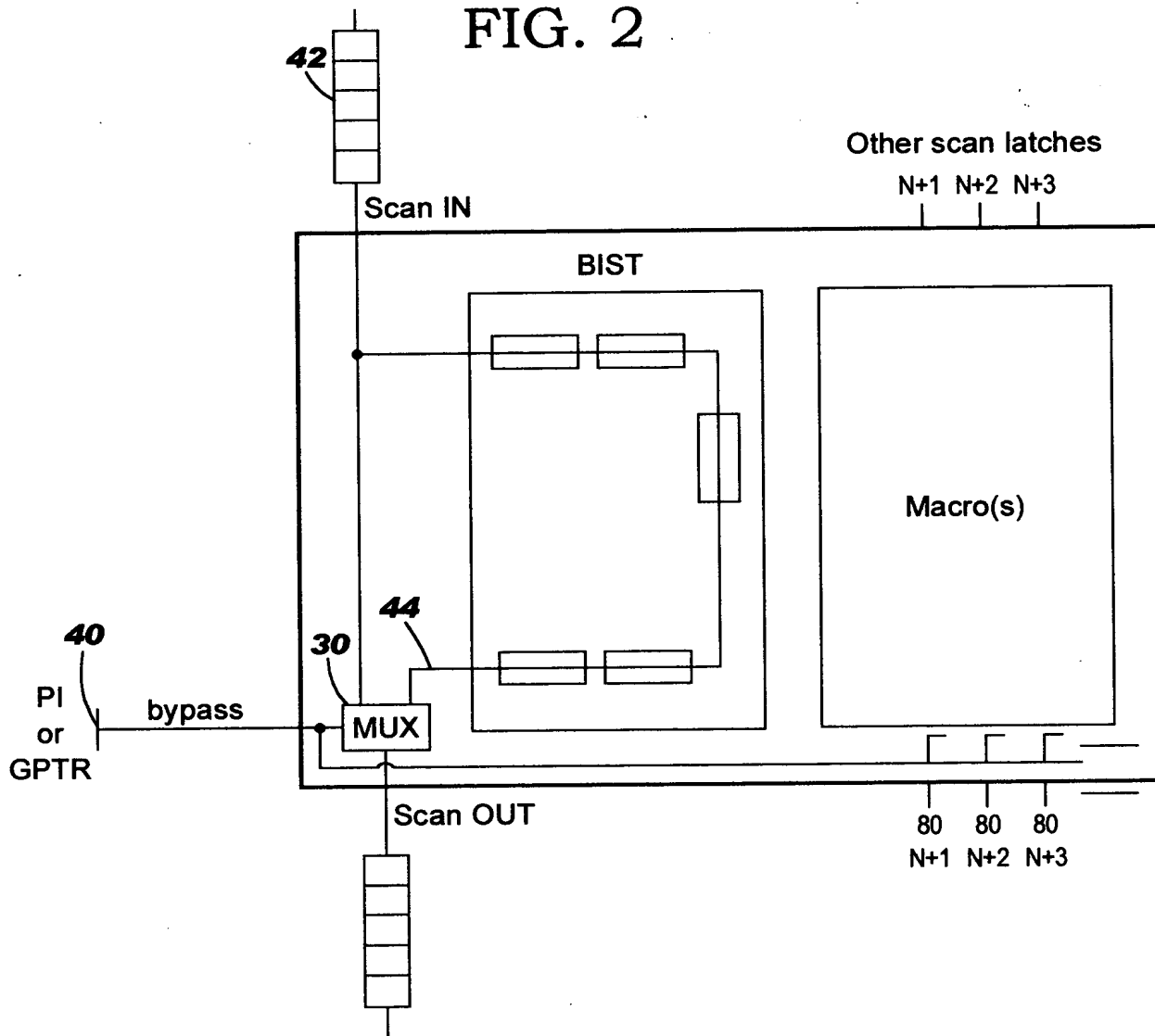


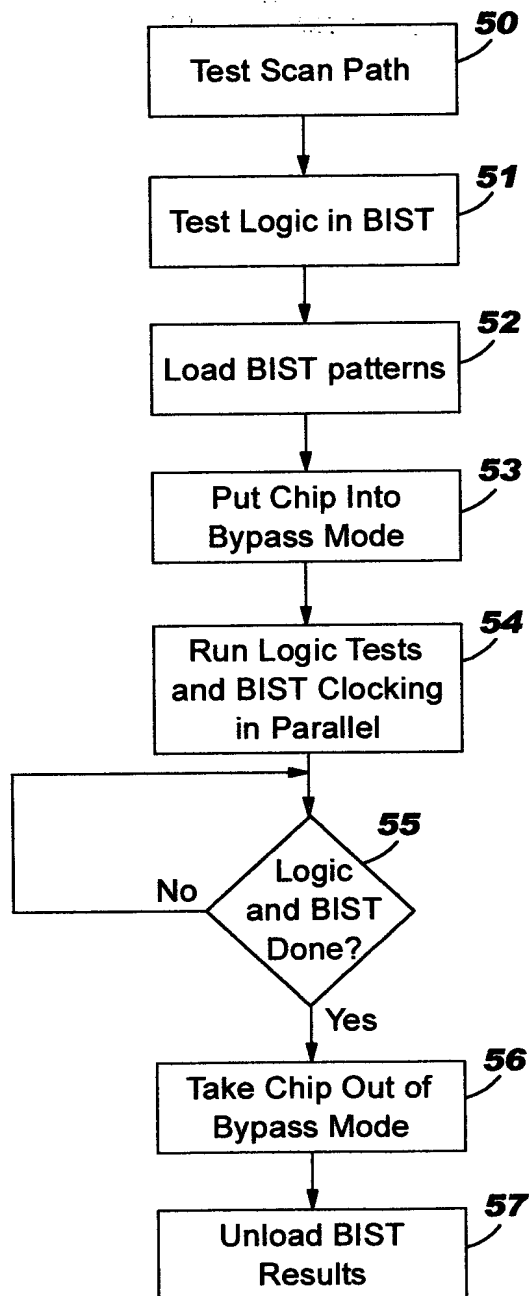
FIG. 2



10065503 122303 202222T 60559001



FIG. 3



1006503 12302
206221 "E0559001